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Alghazo, J.M.

Optimization effects on modeling and synthesis of a conventional floating point fused multiply-add arithmetic unit using CAD tools
(2009) *Journal of Interdisciplinary and Multidisciplinary Research*, 3 (1), .

Abstract
In this paper, a high speed Arithmetic synthesizable Fused Multiply Add Unit (FMA) is modeled capable of implementing the following operations: Addition/subtraction and multiplication. With area speed tradeoff limitation, concentration is on modeling high speed arithmetic units with moderate area increase. Thus, the concentration is on developing units that share the same hardware. A model of a high speed arithmetic fused multiply add unit (A*B +C) Capable of addition/subtraction and multiplication is implemented. The focus is on reducing the delay in critical path by identifying the most time consuming operations in the critical path of a basic multiplication/addition fused unit. CAD tools are used to model this system. Once modeled and synthesized the system is downloaded onto a FPGAs chip. The chip became a stand alone FMA unit capable of implementing the operations mentioned. Synthesis tools are used to evaluate these designs and reports showed that the estimated minimum delay of the designed unit was 112.917ns. After implementing optimization techniques and modeling the FMA unit using Verilog synthesis tools, the estimated the minimum delay of the design unit was 9.236 ns. The efficiency of the system is therefore increased by over a factor of 10.

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